Claims

What is claimed is:

1. A system for monitoring and regulating an etch process, comprising:

at least one etching component operative to etch at least one portion of a wafer;

an etch component driving system for driving the at least one etching component;

a system for directing light toward one or more gratings located on at least one portion of the wafer;

an etch monitoring system operable to measure one or more etching parameters from light reflected from the one or more gratings; and

a processor operatively coupled to the etch monitoring system and the etch component driving system, wherein the processor receives an etching parameter data from the measuring system and analyzes the etching parameter data by comparing the etching parameter data to stored etching data to generate a feed-forward control data operative to control the at least one etching component.

2. The system of claim 1, the etch monitoring system further including a scatterometry system for processing the light reflected from the one or more gratings.

3. The system of claim 2, the processor being operatively coupled to the scatterometry system, the processor analyzing data received from the scatterometry system and producing an analyzed data and the processor controlling, at least in part, the at least one etching component *via* the etching component driving system based, at least in part, on the analyzed data.

4. The system of claim 3, wherein the etch process is at least one of descum etching, PR trim etching, BARC etching and main etching.

5. The system of claim 3, wherein the etch process is at least one of an isotropic etch process and an anisotropic etch process.

6. The system of claim 3, wherein the etch process is a dry-etching process where the mechanism of etching has at least one of a physical basis, a chemical basis and a combination of physical and chemical bases.

7. The system of claim 6, wherein the dry-etching technique with a mechanism of etching as a physical basis is at least one of a glow-discharge sputtering technique and an ion-milling technique.

8. The system of claim 6, wherein the dry-etching technique with a mechanism of etching as a chemical basis is a plasma etching technique.

9. The system of claim 8, wherein the dry-etching technique with a combination of bases is at least one of a reactive ion etching (RIE) technique and an ion-enhanced etching technique.

10. The system of claim 2, the processor logically mapping the wafer into one or more grid blocks and making a determination of the acceptability of etching values in the one or more grid blocks.

11. The system of claim 10, wherein the processor determines the existence of unacceptable etching values for at least a portion of the wafer based on comparing one or more measured etching values to one or more stored etching values.

12. The system of claim 11, wherein the processor employs a non-linear training system in computing feed-forward control data operable to adjust the at least one etching component.

13. A method for monitoring and regulating an etch process comprising:

logically partitioning a wafer into one or more portions;

fabricating one or more gratings to be etched on the wafer;

directing an incident light onto at least one of the one or more gratings;

collecting a reflected light reflected from the at least one grating;

measuring the reflected light to determine one or more critical dimensions associated with the at least one grating;

computing one or more adjustments for one or more etching components by comparing the one or more critical dimensions to scatterometry signatures associated with one or more stored critical dimensions; and

adjusting the etch process based, at least in part, on the one or more adjustments.

14. The method of claim 13, further comprising processing the reflected light in a scatterometry system.

15. The method of claim 14 wherein computing the one or more adjustments is based, at least in part, on data received from the scatterometry system.

16. The method of claim 15, wherein the etch process is regulated for portions of the wafer that have been etched.

17. The method of claim 15 wherein the etch process is regulated for unetched portions on the wafer that have not been etched.

18. The method of claim 15, wherein the etch process is regulated for subsequent wafers.

19. The system of claim 15, wherein the etch process is a dry-etching process where the mechanism of etching has at least one of a physical basis, a chemical basis and a combination of physical and chemical bases.

20. The system of claim 19, wherein the dry-etching technique with a mechanism of etching as a physical basis is at least one of a glow-discharge sputtering technique and an ion-milling technique.

21. The system of claim 19, wherein the dry-etching technique with a mechanism of etching as a chemical basis is a plasma etching technique.

22. The system of claim 19, wherein the dry-etching technique with a combination of bases is at least one of a reactive ion etching (RIE) technique and an ion-enhanced etching technique.

23. A method for monitoring and regulating an etch process comprising:

logically partitioning a wafer into one or more grid blocks;

etching the wafer with one or more etching components, where the one or more etching components are operable to etch at least one of the one or more grid blocks;

directing an incident light on at least one of the one or more grid blocks;

monitoring the etch process in at least one of the one or more grid blocks by analyzing light reflected from the at least one of the one or more grid blocks; and

coordinating control of at least one of the one or more etching components based, at least in part, on the analysis of the light reflected from the at least one of the one or more grid blocks.

24. The method of claim 23, wherein the one or more grid blocks are measured at pre-determined intervals of time.

25. A system for monitoring and regulating an trim process, comprising:

means for partitioning a wafer into one or more grid blocks:

scatterometry means for sensing the acceptability of etching in at least one of the one or more grid blocks;

means for controlling the etching of a wafer portion; and

means for selectively controlling the means for etching.